This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of Claims:

1-36. (Cancelled)

37. (Previously Presented) A process of forming an encapsulated circuit board arrangement having at least one layer of tracks, the encapsulated circuit board arrangement having a first side as an interface side and a second side as a protective cover, the process comprising the steps of:

applying at least one layer of sequentially processed tracks on a first side of an interface carrier, a second side of the interface carrier being an interface side of the encapsulated circuit board arrangement; and

joining a last applied sequentially processed layer to a support carrier with an adhesive layer, the support carrier forming the protective cover of the second side of the encapsulated circuit board arrangement.

38. (Previously Presented) The process according to claim 37, wherein the process further comprises the step of:

applying the adhesive layer on top of the last applied sequentially processed layer.

39. (Previously Presented) The process according to claim 37, wherein the process further comprises the step of:

applying the adhesive layer to the support carrier.

40. (Previously Presented) The process according to claim 37, wherein at least one of the at least one sequentially processed layer is applied using offset printing technology.

41. (Previously Presented) The process according to claim 40, wherein the step of applying at least one layer of sequentially processed tracks comprises the step of applying an acrylate as a dielectric of at least one of the at least one sequentially processed layer.

42. (Previously Presented) The process according to claim 38, wherein the adhesive layer is applied using offset printing technology.

43. (Previously Presented) The process according to claim 37, wherein the step of joining the last applied sequentially processed layer to a support carrier comprises the step of joining the last applied sequentially processed layer to a support carrier which is at least a part of a cover housing in which the encapsulated circuit board arrangement is mounted.

44. (Previously Presented) The process according to claim 37, wherein the step of joining the last applied sequentially processed layer to a support carrier comprises the step of joining the last applied sequentially processed layer to a support carrier which is at least a part of an enclosure on which the encapsulated circuit board arrangement is mounted.

45. (Previously Presented) The process according to claim 37, wherein the step of joining the last applied sequentially processed layer to a support carrier comprises the step of joining the last applied sequentially processed layer to a support carrier which is rigid.

46. (Previously Presented) The process according to claim 37, wherein the step of joining the last applied sequentially processed layer to a support carrier comprises the step of joining the last applied sequentially processed layer to a support carrier which is bendable.

47. (Previously Presented) The process according to claim 37, wherein the step of applying at least one layer of sequentially processed tracks comprises the step of applying at least one sequentially processed layer having connection circuitry.

48. (Previously Presented) The process according to claim 37, wherein the step of applying at least one layer of sequentially processed tracks comprises the step of applying at least one sequentially processed layer having tracks arranged as at least one passive component.

49. (Previously Presented) The process according to claim 37, wherein the step of applying at least one layer of sequentially processed tracks comprises the step of applying at least one sequentially processed layer having tracks arranged as at least one active component.

50. (Previously Presented) The process according to claim 37, wherein the at least one layer of sequentially processed tracks is applied to an interface layer having at least one via.

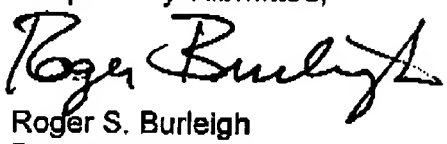
51. (Previously Presented) The process according to claim 37, wherein the at least one layer of sequentially processed tracks is applied to an interface layer having at least one solid via.

52. (Previously Presented) The process according to claim 37, wherein the at least one layer of sequentially processed tracks is applied to an interface layer that is bendable.

53. (Previously Presented) The process according to claim 37, wherein the at least one layer of sequentially processed tracks is applied to an interface layer that is made of polymide.

54-72. (Cancelled).

Respectfully submitted,



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